If Examiner were to agree with the Board's position to the effect that claims 139-142 would have been obvious over Franke, Applicant requests of Examiner to explain how he would propose to modify Franke in such manner at to attain the claimed invention as it is expressly defined in and by claims 139-142. Also, Examiner would need to provide an explanation as to what would motivate a skilled artisan to seek to modify Franke in such exact manner as to attain the claimed invention.

Otherwise and inter alia, Applicant believes new claims 145-146 to be patentable over the cited prior art for the following reasons.

(a) Claims 145-146 both specify details with respect to the waveforms of the transistor driving voltages as well as the (emitter-to-collector) current flowing through the transistors. None of the cited references provide for or suggest such driving voltages and waveforms.

(b) Claim 146 additionally provides for a feature whereby the magnitude of the power supplied to the load is controlled by way of controlling the inversion frequency; which feature is neither described nor suggested by any of the cited references.

Ole K. Nilssen, Pro Se Applicant

312-658-5615

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AMENDED CLAIMS in Serial No. 06/787,692

139. (Amended) The combination of:

rectifier means: i) connected with an ordinary electric utility power line by way of a first and a second AC input terminal, and ii) operative to provide a DC voltage at a DC output;

self-oscillating inverter circuit connected with said DC output and operative to provide a sinusoidal output voltage of relatively high frequency across a pair of AC output terminals, one of the AC output terminals being electrically connected with the first AC input terminal by way of a linear conductance means, such as a plain electric conductor, the inverter-circuit comprising an L-C circuit: i) having a capacitor and an inductor, ii) being connected in circuit with the AC output terminals in such manner that the capacitor is effectively connected across the AC output terminals, and iii) being resonant at or near said relatively high frequency; and

load means connected with the AC output terminals and operative to absorb most of the power being provided therefrom.

140. (Amended) The combination of:

rectifier means connected with an ordinary electric utility power line by way of a first and a second AC input terminal and operative to provide a DC voltage at a DC output;

self-oscillating inverter circuit connected with said DC output and operative to provide a sinusoidal output voltage of relatively high frequency across a load means connected with a pair of AC output terminals, the load means being operative to absorb most of the power being provided from the AC output terminals, one of the AC output terminals being at all times at substantially the same electrical potential as that of the first AC input terminal, the inverter circuit comprising an L-C tank circuit connected in circuit with the AC output terminals and having a capacitor and an inductor, the L-C tank circuit being resonant at or near said relatively high frequency, one terminal of the capacitor being connected with the first AC output terminal.

141. (Amended) The combination of:

rectifier means: i) connected with an ordinary electric utility power line by way of a first and a second AC input terminal, and ii) operative to provide a DC voltage at a DC output;

self-oscillating inverter connected with said DC output and operative to provide a substantially squarewave output voltage of relatively high frequency across a pair of squarewave output terminals, one of the squarewave output terminals being electrically connected with the first AC input terminal <u>by way of a substantially linear conductance means, such as a plain electrical conductor</u>, the inverter-circuit comprising an L-C series-circuit: i) having a capacitor and an inductor, ii) being connected with the squarewave output terminals in such manner that one of the terminals of the capacitor is connected with the first AC input terminal, iv) having a load means connected across the capacitor, and v) being resonant at or near said relatively high frequency, thereby to provide a substantially sinusoidal high-frequency voltage across the load means, which load means is operative to absorb most of the real power being provided from the squarewave output terminals.

142. (Amended) In a self-oscillating inverter adapted to be powered from a DC source having a center-tap and to provide an essentially squarewave voltage output, the DC source being connected with and powered from an ordinary electric utility power line by way of a pair of supply conductors, the center-tap being electrically connected <u>without any intervening non-linear impedance means</u> with one of the supply conductors, the inverter comprising a pair of alternatingly conducting switching transistors connected by way of a mid-point in series across the DC source, the squarewave voltage output being provided between the center-tap and the mid-point, the improvement comprising:

a series-connected combination of an inductor and a capacitor connected between the center-tap and the mid-point, the series-connected combination: i) having one of the terminals of its capacitor connected with the center-tap, ii) having a natural resonance frequency equal to or near the fundamental frequency of the squarewave voltage output, and iii) being operative to provide a substantially sinusoidal voltage across a load means effectively connected in parallel with the capacitor, the load means being operative to absorb most of the real power being provided from the squarewave voltage output.

Claims 143 and 144 are cancelled.

145. An arrangement comprising:

rectifier means connected with an ordinary electric utility power line and operative to provide a DC voltage across a set of DC terminals;

an inverter means including a first and a second transistor; the first transistor having a first common terminal, a first control terminal, and a first output terminal; the second transistor having a second common terminal, a second control terminal, and a second output terminal; each transistor being considered as switched ON whenever current if permitted to flow freely in one direction between its common terminal and its output terminal; each transistor being considered as switched OFF when current is not free to flow in said one direction between its common terminal and its output terminal; each transistor existing in a state of being switched ON as long as an ON-voltage is being provided at its control terminal; each transistor existing in a state of being switched OFF as long as an OFF-voltage is being provided at its control terminal; the inverter means being connected with the DC terminals and operative to provide an inverter output voltage across a pair of inverter output terminals in response to a first and a second drive signal provided respectively to the first and second control terminals; each control signal having a fundamental frequency equal to that of the inverter output voltage and, periodically and alternatingly, providing said ON-voltage and OFF-voltage to the control terminal of its associated transistor; the first transistor existing in its state of being switched ON only during periods when the second transistor exists in its state of being switched OFF; the second transistor existing in its state of being switched ON only during periods when the first transistor exists in its state of being switched OFF;

an L-C series-circuit having a tank-capacitor and a tank-inductor; the L-C series-circuit being effectively connected across the inverter output terminals, thereby to cause an inverter output current to flow therebetween; the L-C series-circuit having a natural resonance frequency lower than said fundamental frequency; the waveshape of the inverter output current being substantially sinusoidal and having a fundamental period; a load means being connected in parallel circuit with the tank-capacitor; and

drive signal source connected in circuit with the inverter means and operative to provide the first and second drive signals to the first and second control terminals, respectively; thereby correspondingly to cause each transistor periodically to alternate between the state of being switched ON and the state of being switched OFF; each transistor existing in its state of being switched ON for a first duration during each fundamental period; the first duration being substantially shorter than half of the complete duration of said fundamental period; the inverter output current thereby flowing between the first common terminal and the first output terminal during this first duration but not at any time during the remainder of the complete duration of each fundamental period.

146. An arrangement comprising:

rectifier means connected with an ordinary electric utility power line and operative to provide a DC voltage at a set of DC terminals; the set of DC terminals including a B- terminal and a B+ terminal;

an inverter means including a first and a second transistor effectively connected in series between the B- and the B+ terminals; the first transistor having a first common terminal, a first control terminal, and a first output terminal; the second transistor having a second common terminal, a second control terminal, and a second output terminal; each transistor being considered as switched ON whenever current if permitted to flow freely in one direction between its common terminal and its output terminal; each transistor being considered as switched OFF when current is not free to flow in said one direction between its common terminal and its output terminal; each transistor existing in a state of being switched ON as long as an ON-voltage is being provided at its control terminal; each transistor existing in a state of being switched OFF as long as an OFF-voltage is being provided at its control terminal; the inverter means being connected with the DC terminals and operative to provide an inverter output voltage across a pair of inverter output terminals in response to a first and a second drive signal provided respectively to the first and second control terminals; each control signal having a fundamental frequency equal to that of the inverter output voltage and, periodically and alternatingly, providing said ON-voltage and OFF-voltage to the control terminal of its associated transistor; the first transistor existing in its state of being

switched ON only during periods when the second transistor exists in its state of being switched OFF; the second transistor existing in its state of being switched ON only during periods when the first transistor exists in its state of being switched OFF;

an L-C series-circuit having a tank-capacitor and a tank-inductor; the L-C series-circuit being effectively connected across the inverter output terminals, thereby to cause an inverter output current to flow therebetween; the L-C series-circuit having a natural resonance frequency lower than said fundamental frequency; the waveshape of the inverter output current being substantially sinusoidal and having a fundamental period; a load means being connected in parallel circuit with the tank-capacitor;

drive signal source connected in circuit with the inverter means and operative to provide the first and second drive signals to the first and second control terminals, respectively; thereby correspondingly to cause each transistor, periodically to alternate between the state of being switched ON and the state of being switched OFF; each transistor existing in its state of being switched ON for a first duration during each fundamental period; the first duration being substantially shorter than half of the complete duration of said fundamental period; the inverter output current thereby flowing between the first common terminal and the first output terminal during this first duration but not at any time during the remainder of the complete duration of each fundamental period; and

means connected in circuit with the drive source means and operative to control the amount of power delivered to the load means by way of controlling the frequency of the inverter output voltage.